ABSTRACT

An integrated circuit arrangement clocked by a single clock having variable delays to different regions of said arrangement such that said regions are partially synchronized to each other, the arrangement comprising: a data transfer buffer for buffering a data stream for transfer between respective first and second ones of said regions, and a data transfer controller, associated with said data transfer buffer and said respective regions, configured to control transfer of said data stream by: initially synchronizing between said respective regions at a start of said data stream, receiving data, in said buffer, from said first region, at a predetermined rate, and outputting said data stream to said second region at said predetermined rate in accordance with said initial synchronization. The arrangement allows deterministic data patterns to arrive at the receiving domain at minimal hardware cost.